UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,551	03/31/2004	Nasser A. Kurd	INTEL-0054	4115

34610 7590 06/17/2005

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,551	KURD ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-26 are presented in the instant application according to the Applicants' filing on 03/31/2004.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Sato (JP Patent No. JP02003298417A).

With respect to claim 12, Sato discloses, in Fig. 1, a clocking system comprising a phase lock loop device [2] powered by an analog power supply voltage [5b] and a digital power supply voltage [6b], the phase lock loop device to receive a first clock signal [4] and to output a second clock signal [9b] having an frequency based on a voltage of the digital power supply voltage.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 9-11 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (U.S. Patent No. 6,218,876) in view of Mano et al. (U.S. Patent No. 6,570,456).

With respect to claim 1, Sung et al. discloses, in Fig. 1, a clock generating apparatus comprising a first phase lock loop device [52] and a second phase lock loop device [54].

Sung et al. fails to disclose details of the first and second phase locked loop devices with first and second power supply voltages.

Mano et al. discloses, in Fig. 1, a phase locked loop with first and second power supply voltages.

The combined teaching of Sung et al. and Mano et al. discloses a clock generating apparatus comprising a first phase lock loop device [Sung et al.'s, Fig. 1, item 52 as with details

in Mano et al.'s, Fig. 1, item L21] to be powered by a first power supply voltage [Vdd *(not shown since it is inherent for a PLL to be powered by a power supply voltage to operate)*], and a second phase lock loop device [Sung et al.'s, Fig. 1, item 54 as with details in Mano et al.'s, Fig. 1, item L21], coupled to the first phase lock loop device, to be powered by the first power supply voltage [Vdd *(not shown since it is inherent for a PLL to be powered by a power supply voltage to operate)*] and a second power supply voltage [V11], the second phase lock loop device to output a clock signal having an adaptive frequency based on the second power supply voltage.

To configure the circuit of Sung et al. with a detailed phase locked loop as taught by Mano et al. to provide clock signals that are stable phase synchronous with the reference signal would have been obvious to one of ordinary skill in the art at the time of the invention since Mano et al. teaches that regardless of the variation in the manufacturing parameter, the frequency characteristics can be adjusted as to compensate for the variation *(see Mano et al., col. 5, lines 33-41)*.

With respect to claim 2, the combined teaching of Sung et al. and Mano et al. discloses that the first power supply voltage comprises an analog voltage [Vdd] and the second power supply comprises a digital voltage [V11].

With respect to claim 3, the combined teaching of Sung et al. and Mano et al. discloses that the frequency of the clock signal output from the second phase lock loop device are based on fluctuations of the second power supply voltage [V11].

With respect to claim 4, the combined teaching of Sung et al. and Mano et al. discloses that the first phase lock loop device outputs a clock signal having a fixed frequency, the clock signal having the fixed frequency being input to the second phase lock loop device.

With respect to claim 5, the combined teaching of Sung et al. and Mano et al. discloses that the second phase lock loop device includes components powered by the first power supply voltage and components powered by the second power supply voltage.

With respect to claim 6, the combined teaching of Sung et al. and Mano et al. discloses that the second phase lock loop device includes a voltage controlled oscillator (VCO) powered by the second power supply voltage [V11].

With respect to claim 7, the combined teaching of Sung et al. and Mano et al. discloses that a sensitivity to droop is based on a coupling percentage of the second power supply voltage to power the VCO.

With respect to claim 9, the combined teaching of Sung et al. and Mano et al. discloses that a sensitivity to voltage droop is determined based on a ratio of transistor sizes within the second phase lock loop device *[Sung et al.'s, Fig. 1, item 54 as with details in Mano et al.'s, Fig. 1, items MC21, M25, M26, MC22].*

With respect to claim 10, the combined teaching of Sung et al. and Mano et al. discloses that the apparatus corrects for phase error accumulation.

With respect to claim 11, the combined teaching of Sung et al. and Mano et al. further discloses that buffers to couple core components, operating based on the clock signal, with external I/0 [Sung et al.'s Figs. 1 and 5].

With respect to claim 22, Sung et al. discloses, in Figs. 1 and 5, an electronic system comprising an integrated circuit having a clock generating apparatus and I/O components coupled external to the integrated circuit, the clock generating circuit comprising a first phase lock loop device [52] and a second phase lock loop device [54].

Sung et al. fails to disclose details of the first and second phase locked loop devices with first and second power supply voltages.

Mano et al. discloses, in Fig. 1, a phase locked loop with first and second power supply voltages.

The combined teaching of Sung et al. and Mano et al. discloses a clock generating apparatus comprising a first phase lock loop device [Sung et al.'s, Fig. 1, item 52 as with details in Mano et al.'s, Fig. 1, item L21] to be powered by a first power supply voltage [Vdd *(not shown since it is inherent for a PLL to be powered by a power supply voltage to operate)*], and a second phase lock loop device [Sung et al.'s, Fig. 1, item 54 as with details in Mano et al.'s, Fig. 1, item L21], coupled to the first phase lock loop device, to be powered by the first power supply voltage [Vdd *(not shown since it is inherent for a PLL to be powered by a power supply voltage to operate)*] and a second power supply voltage [V11], the second phase lock loop device to output a clock signal having an adaptive frequency based on the second power supply voltage.

To configure the circuit of Sung et al. with a detailed phase locked loop as taught by Manu et al. to provide clock signals that are stable phase synchronous with the reference signal would have been obvious to one of ordinary skill in the art at the time of the invention since Mano et al. teaches that regardless of the variation in the manufacturing parameter, the frequency characteristics can be adjusted as to compensate for the variation *(see Mano et al., col. 5, lines 33-41)*.

With respect to claim 23, the combined teaching of Sung et al. and Mano et al. discloses that the first power supply voltage comprises an analog voltage [Vdd] and the second power supply comprises a digital voltage [V11].

With respect to claim 24, the combined teaching of Sung et al. and Mano et al. discloses that the frequency of the clock signal output from the second phase lock loop device are based on fluctuations of the second power supply voltage [V11].

With respect to claim 25, the combined teaching of Sung et al. and Mano et al. further discloses that buffers to couple core components, operating based on the clock signal, with external I/0 [Sung et al.'s Figs. 1 and 5].

With respect to claim 26, the combined teaching of Sung et al. and Mano et al. discloses that the first power supply and the second power supply are external to the integrated circuit.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (U.S. Patent No. 6,218,876) in view of Mano et al. (U.S. Patent No. 6,570,456), as applied in claim 1, and further in view of Delbo' et al. (U.S. Patent No. 6,816,019).

The combined teaching of Sung et al. and Mano et al. discloses all the claimed limitations as expressly recited in claim 1 including the second detailed phase locked loop (*with a disclosed low pass filter in Mano et al., Fig. 1, item LP2*), except for a sensitivity to voltage droop is determined based on a ratio of capacitor sizes within the second phase lock loop device.

Delbo' et al. discloses a low pass filter, in Fig. 3, with a low pass filter having two capacitors [cf1, cf2].

To configure a circuit based on the combined teaching of Sung et al. and Mano et al. with a low pass filter as taught by Delbo' et al. so that a voltage signal can be input to the voltage controlled oscillator and an desired frequency can be obtain would have been obvious to one of ordinary skill in the art at the time of the invention since Delbo'et al. teaches that such low pass

filter could provide a damping factor such that the transient of the PLL system can be fast and does not show any overshoots *(see Delbo'et al. col. 2, lines 28-33).*

7. Claims 13-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (JP Patent No. 02003298417A) in view of Sung et al. (U.S. Patent No. 6,218,876).

With respect to claim 13, Sato discloses all the claimed limitations as expressly recited in claim 12, except for the clocking system further comprising a fixed phase lock loop device powered by the analog power supply voltage, the fixed phase lock loop device to receive a reference clock signal and to provide the first clock signal to the adaptive phase lock loop device.

Sung et al. discloses, in Fig. 1, a phase locked loop circuitry that includes two serially connected PLL devices [52, 54], with a first/fixed phase lock loop device [52] to receive a reference clock signal [20] and to provide the first clock signal to the second/adaptive phase lock loop device [54].

To configure the circuit of Sato et al. in an arrangement having two serially connected PLL devices as taught by Sung et al. to provide frequencies in a narrower range would have been obvious to one of ordinary skill in the art at the time of the invention since Sung et al. teaches that by doing so the PLL circuit can operate in a narrower range than might otherwise be required to produce a given input-to-final frequency change *(see Sung et al., abs., lines 11-14).*

With respect to claim 14, the combined teaching of Sato and Sung et al. discloses that fluctuations of the frequency of the second clock signal are based on fluctuations of the digital power supply voltage.

With respect to claim 15, the combined teaching of Sato and Sung et al. discloses that the fixed phase lock loop device outputs the first clock signal having a fixed frequency.

With respect to claim 16, the combined teaching of Sato and Sung et al. discloses that the adaptive phase lock loop device includes components powered by the analog power supply voltage [5b] and components powered by the digital power supply voltage [6b].

With respect to claim 17, the combined teaching of Sato and Sung et al. discloses that the adaptive phase lock loop device includes a voltage-controlled oscillator (VCO) powered by the digital power supply voltage.

With respect to claim 18, the combined teaching of Sato and Sung et al. discloses that a sensitivity to droop is based on a coupling percentage of the second power supply voltage to power the VCO.

With respect to claim 20, the combined teaching of Sato and Sung et al. discloses that a sensitivity to voltage droop is determined based on a ratio of transistor sizes within the adaptive phase lock loop device.

With respect to claim 21, the combined teaching of Sato and Sung et al. further discloses buffers to couple core components with external I/0 [Sung et al.'s Figs. 1 and 5].

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (JP Patent No.02003298417A) in view of Mano et al. (U.S. Patent No. 6,570,456), as applied in claim 12, and further in view of Delbo' et al. (U.S. Patent No. 6,816,019).

The combined teaching of Sato and Mano et al. discloses all the claimed limitations as expressly recited in claim 12. Sung et. al. also discloses, in Fig. 3, a phase locked loop having a low-pass filter.

The combined teaching of Sato and Mano et al. fails to teach a sensitivity to voltage droop is determined based on a ratio of capacitor sizes within the second phase lock loop device.

Delbo' et al. discloses a low pass filter, in Fig. 3, with a low pass filter having two capacitors [cf1, cf2].

To configure a circuit based on the combined teaching of Sato and Sung et al. with a low pass filter as taught by Delbo' et al. so that a voltage signal can be input to the voltage controlled oscillator and an desired frequency can be obtain would have been obvious to one of ordinary skill in the art at the time of the invention since Delbo'et al. teaches that such low pass filter could provide a damping factor such that the transient of the PLL system can be fast and does not show any overshoots *(see Delbo'et al. col. 2, lines 28-33)*.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER